In the Specification:

Please insert before the first paragraph of the application:

This application is the national stage application of international application number PCT/DE03/003552, filed on October 24, 2003, which claims the benefit of priority to German Patent Application 102 50 204.8, filed on October 28, 2002, incorporated herein by reference.

Please rewrite the paragraphs on page 7, lines 5-27 as follows:

A full trench is a trench, for example between components of a chip, in which the silicon is etched or interrupted as far as the buried layers, so that current paths between the components are completely interrupted. A full trench can isolate relatively large transistor regions from one another, as is also described in an article by S. Maeda, "Impact of 0.18 μm SOI CMOS Technology using Hybrid Trench Isolation with High Resistivity Substrate on Embedded RF/Analog Applications", 2000 Symp. on VLSI Technology - Digest of Technical Papers (CAT. No. 00CH37104), pages 154 to 155, hereby incorporated by reference.

A deep trench is described for example in the article "An SOI-Based High Performance Self-Aligned Bipolar Technology Featuring 20 ps Gate-Delay and a 8.6 fJ Power Delay Product" by E. Bertagnolli et al., 1993, Symp. on VLSI Technology, Digest of Technical Papers (CAT. No. 93CH3303-5), pages 63 to 64, hereby incorporated by reference. In contrast to the full trench, the deep trench is not wide enough to be able to integrate the entire dimensions of passive components above it. Rather, the deep trench serves for dielectric component isolation.

Please rewrite the paragraphs on page 9, line 37-page 10, line 19 as follows:

The openings 12 are etched into an STI oxide layer 13 down to the second auxiliary layer 7, which STI oxide layer preferably covers the whole area of the semiconductor substrate 1 with the auxiliary layers 6 and 7 situated thereon. As is known from EP 0 600 276 B1, hereby incorporated

by reference, the etching may be effected by anisotropic dry etching which stops selectively on silicon nitride, and thus on the second auxiliary layer 7.

In the subsequent method step in accordance with figure 1b, a lateral undercut 14 of the auxiliary layers 6 and 7 is effected. The undercut 14 is described in more detail in EP 0 600 276 B1, hereby incorporated by reference. Since sidewall defects form proceeding from the interfaces between the auxiliary layers 6 and 7 and the surface of the buried layers 5.1 and 5.2 and grow up at an angle of about 52° along (111) crystal faces, that is to say for example along the sidewall of the STI oxide layer, this growth of the sidewall defects can be interrupted by the overhang formed by the undercuts 14 of the STI oxide layer 13.